Data Sheet | May 19, 2008 | FN7436.7

Micropower Single Supply Rail-to-Rail Input-Output Precision Op Amp

The EL8176 is a precision low power, operational amplifier. The device is optimized for single supply operation between 2.4V to 5.5V.

The EL8176 draws minimal supply current while meeting excellent DC-accuracy noise and output drive specifications. Competing devices seriously degrade these parameters to achieve micropower supply current.

The EL8176 can be operated from one lithium cell or two Ni-Cd batteries. The input range includes both positive and negative rail. The output swings to both rails

Ordering Information

PART NUMBER	PART MARKING	PACKAGE (Pb-Free)	PKG. DWG. #
EL8176FWZ-T7* (Note 1)	BBVA	6 Ld SOT-23	MDP0038
EL8176FWZ-T7A* (Note 1)	BBVA	6 Ld SOT-23	MDP0038
EL8176FSZ (Note 1)	8176FSZ	8 Ld SO	MDP0027
EL8176FSZ-T7* (Note 1)	8176FSZ	8 Ld SO	MDP0027
EL8176FIZ-T7* (Note 2)	176Z	6 Ld WLCSP (1.5mmx1.0mm)	W3x2.6C

*Please refer to TB347 for details on reel specifications.

NOTES:

1. These Intersil Pb-free plastic packaged products employ special Pb-free material sets, molding compounds/die attach materials, and 100% matte tin plate plus anneal (e3 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations). Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.
2. These Intersil Pb-free WLCSP and BGA packaged products products employ special Pb-free material sets; molding compounds/die attach materials and SnAgCu - e1 solder ball terminals, which are RoHS compliant and compatible with both SnPb and Pb-free soldering operations. Intersil Pb-free WLCSP and BGA packaged products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.

Features

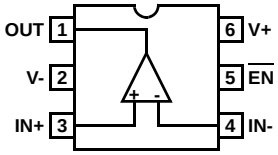
- 55µA supply current
- 100µV max offset voltage (8 Ld SO)
- 2nA input bias current
- 400kHz gain-bandwidth product
- Single supply operation down to 2.4V
- Rail-to-rail input and output
- Output sources 31mA and sinks 26mA load current
- Pb-free plus (RoHS compliant)

Applications

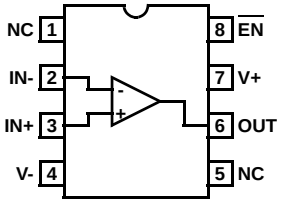
- Battery- or solar-powered systems
- 4mA to 20mA current loops
- Handheld consumer products
- Medical devices
- Thermocouple amplifiers
- Photodiode pre amps
- pH probe amplifiers

Pinouts

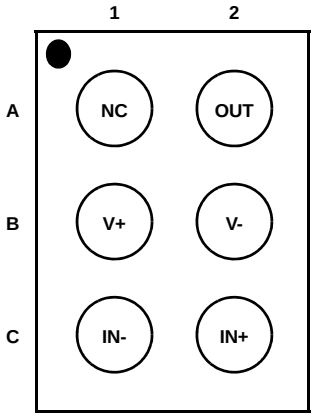
EL8176
(6 LD SOT-23)
TOP VIEW



EL8176
(8 LD SO)
TOP VIEW



EL8176
(6 LD WLCSP)
TOP VIEW



Absolute Maximum Ratings (T_A = +25°C)

Supply Voltage (V_S) and Pwr-up Ramp Rate 5.75V, 1V/µs
Differential Input Voltage 0.5V
Current into IN+, IN-, and $\overline{EN}$. 5mA
Input Voltage . . . . . V- - 0.5V to V+ + 0.5V
ESD Tolerance
Human Body Model 3kV
Machine Model 300V

Thermal Information

Thermal Resistance (Typical, Note 3)	θ_{JA} (°C/W)
6 Ld SOT-23 Package	230
6 Ld WLCSP Package	130
8 Ld SO Package	125

Ambient Operating Temperature Range . . . . . -40°C to +125°C
Storage Temperature Range . . . . . -65°C to +150°C
Operating Junction Temperature . . . . . +125°C
Pb-free reflow profile . . . . . .see link below
http://www.intersil.com/pbfree/Pb-FreeReflow.asp

CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions may adversely impact product reliability and result in failures not covered by warranty.

NOTES:

3. θ_{JA} is measured with the component mounted on a high effective thermal conductivity test board in free air. See Tech Brief TB379 for details.

IMPORTANT NOTE: All parameters having Min/Max specifications are guaranteed. Typical values are for information purposes only. Unless otherwise noted, all tests are at the specified temperature and are pulsed tests, therefore: $T_J = T_C = T_A$

Electrical Specifications

V_+ = 5V, V_- = 0V, V_{CM} = 2.5V, R_L = Open, V_{EN} = 0V, T_A = +25°C unless otherwise specified. **Boldface limits apply over the operating temperature range, -40°C to +125°C.** Temperature data established by characterization.

PARAMETER	DESCRIPTION	CONDITIONS	MIN (Note 4)	TYP	MAX (Note 4)	UNIT
DC SPECIFICATIONS						
V_{OS}	Input Offset Voltage	8 Ld SO	-100	±25	100	µV
			-220		**220**	µV
		6 Ld SOT-23	-350	±80	350	µV
			-350		**350**	µV
		WLCSP	**-500**	-75	**500**	µV
$\frac{\Delta V_{OS}}{\Delta Time}$	Long Term Input Offset Voltage Stability			2.4		µV/Mo
$\frac{\Delta V_{OS}}{\Delta T}$	Input Offset Drift vs Temperature			0.7		µV/°C
I_{OS}	Input Offset Current		-1	±0.4	1	nA
			-4		**4**	nA
I_B	Input Bias Current		-2	±0.5	2	nA
			-5		**5**	nA
CMIR	Input Voltage Range	Guaranteed by CMRR test	0		5	V
CMRR	Common-Mode Rejection Ratio	V_{CM} = 0V to 5V	90	110		dB
			90			dB
PSRR	Power Supply Rejection Ratio	V_S = 2.4V to 5.5V	90	110		dB
			90			dB
A_{VOL}	Large Signal Voltage Gain	V_O = 0.5V to 4.5V, R_L = 100kΩ	200	500		V/mV
			200			V/mV
		V_O = 0.5V to 4.5V, R_L = 1kΩ		25		V/mV

Electrical Specifications $V_+ = 5V$, $V_- = 0V$, $V_{CM} = 2.5V$, R_L = Open, $V_{EN} = 0V$, $T_A = +25°C$ unless otherwise specified. **Boldface limits apply over the operating temperature range, -40°C to +125°C.** Temperature data established by characterization. **(Continued)**

PARAMETER	DESCRIPTION	CONDITIONS	MIN (Note 4)	TYP	MAX (Note 4)	UNIT
V_{OUT}	Maximum Output Voltage Swing SOT-23/SO-8	VOL; Output low, $R_L = 100k\Omega$		3	8	mV
					10	mV
		VOL; Output low, $R_L = 1k\Omega$		130	200	mV
					300	mV
		VOH; Output high, $R_L = 100k\Omega$	4.994	4.997		V
			4.992			V
		VOH; Output high, $R_L = 1k\Omega$	4.750	4.867		V
			4.7			V
	Maximum Output Voltage Swing WLCSP	VOL; Output low, $R_L = 100k\Omega$		3	8	mV
					10	mV
		VOL; Output low, $R_L = 1k\Omega$		130	200	mV
					300	mV
		VOH; Output high, $R_L = 100k\Omega$	**4.991**	4.997		V
		VOH; Output high, $R_L = 1k\Omega$	4.750	4.867		V
			4.7			V
$I_{S,ON}$	Supply Current, Enabled	$V_{EN} = 5V$, SOT-23/SO-8	35	55	75	µA
			30		**90**	µA
		$V_{EN} = 5V$, WLCSP	60	85	110	µA
			55		**120**	µA
$I_{S,OFF}$	Supply Current, Disabled	$V_{EN} = 0V$, SOT-23/SO-8 only		3	10	µA
					10	µA
I_O+	Short Circuit Output Sourcing Current	$R_L = 10\Omega$	18	31		mA
			18			mA
I_O-	Short Circuit Output Sinking Current	$R_L = 10\Omega$	17	26		mA
			15			mA
V_S	Supply Voltage	Guaranteed by PSRR test	2.4		5.5	V
			2.4		**5.5**	V
V_{INH}	Enable Pin High Level	SOT-23 and SO packages only	2			V
V_{INL}	Enable Pin Low Level	SOT-23 and SO packages only			0.8	V
I_{ENH}	Enable Pin Input Current	$V_{EN} = 5V$, SOT-23 and SO packages only	0.25	0.7	2.0	µA
					2.5	µA
I_{ENL}	Enable Pin Input Current	$V_{EN} = 0V$, SOT-23 and SO packages only	-0.5	0	+0.5	µA
			-1		**+1**	µA
AC SPECIFICATIONS						
GBW	Gain Bandwidth Product	$A_V = 100$, $R_F = 100k\Omega$, $R_L = 10k\Omega$, $R_G = 1k\Omega$ to V_{CM}		400		kHz
Unity Gain Bandwidth	-3dB Bandwidth	$A_V = 1$, $R_F = 0\Omega$, $R_L = 100k\Omega$ to V_{CM}, $V_{OUT} = 10mV_{P-P}$		1		MHz

Electrical Specifications $V_+ = 5V$, $V_- = 0V$, $V_{CM} = 2.5V$, R_L = Open, $V_{EN} = 0V$, $T_A = +25°C$ unless otherwise specified. **Boldface limits apply over the operating temperature range, -40°C to +125°C.** Temperature data established by characterization. **(Continued)**

PARAMETER	DESCRIPTION	CONDITIONS	MIN (Note 4)	TYP	MAX (Note 4)	UNIT
e_N	Input Noise Voltage Peak-to-Peak	f = 0.1Hz to 10Hz, R_L = 10kΩ to V_{CM}		1.5		μV_{P-P}
	Input Noise Voltage Density	f_O = 1kHz		28		nV/√Hz
i_N	Input Noise Current Density	f_O = 1kHz		0.16		pA/√Hz
ISO	Off-State Input to Output Isolation	V_{EN} = 5V, f_O = 1kHz, A_V = +1, $V_{IN} = 1V_{P-P}$ SOT-23 and SO packages only		-73		dB
CMRR	Input Common Mode Rejection Ratio	f_O = 120Hz; $V_{CM} = 1V_{P-P}$,		-70		dB
PSRR+	Power Supply Rejection Ratio (V_+)	f_O = 120Hz; V_+, V_- = ±2.5V, $V_{SOURCE} = 1V_{P-P}$		-90		dB
PSRR-	Power Supply Rejection Ratio (V_-)	f_O = 120Hz; V_+, V_- = ±2.5V, $V_{SOURCE} = 1V_{P-P}$		-70		dB
TRANSIENT RESPONSE						
SR	Slew Rate		**±0.065**	±0.13	**±0.3**	V/µs
t_r, t_f, Large Signal	Rise Time, 10% to 90%, V_{OUT}	A_V = +2, $V_{OUT} = 2V_{P-P}$, $R_g = R_f = R_L$ = 10kΩ to V_{CM}		18		µs
	Fall Time, 90% to 10%, V_{OUT}	A_V = +2, $V_{OUT} = 2V_{P-P}$, $R_g = R_f = R_L$ = 10kΩ to V_{CM}		19		µs
t_r, t_f, Small Signal	Rise Time, 10% to 90%, V_{OUT}	A_V = +2, $V_{OUT} = 10mV_{P-P}$, $R_g = R_f = R_L$ = 10kΩ to V_{CM}		2.4		µs
	Fall Time, 90% to 10%, V_{OUT}	A_V = +2, $V_{OUT} = 10mV_{P-P}$, $R_g = R_f = R_L$ = 10kΩ to V_{CM}		2.4		µs
$t_{\overline{EN}}$	$\overline{EN}$ to Output Turn-on Delay Time, 10% $\overline{EN}$ to 10% V_{OUT} (SOT-23, SO packages)	$V_{\overline{EN}}$ = 5V to 0V, A_V = +2, $R_g = R_f = R_L$ = 10kΩ to V_{CM}		4		µs
	$\overline{EN}$ to Output Turn-off Delay Time, 10% $\overline{EN}$ to 10% V_{OUT} (SOT-23, SO packages)	$V_{\overline{EN}}$ = 0V to 5V, A_V = +2, $R_g = R_f = R_L$ = 10kΩ to V_{CM}		0.1		µs

NOTE:

4. Parameters with MIN and/or MAX limits are 100% tested at +25°C, unless otherwise specified. Temperature limits established by characterization and are not production tested.

Typical Performance Curves

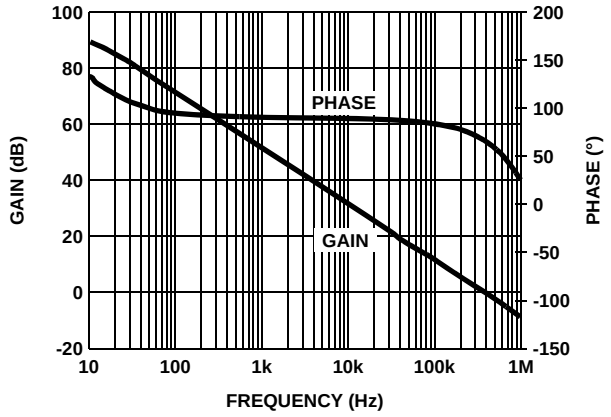


FIGURE 1. A_{VOL} vs FREQUENCY @ 1kΩ LOAD

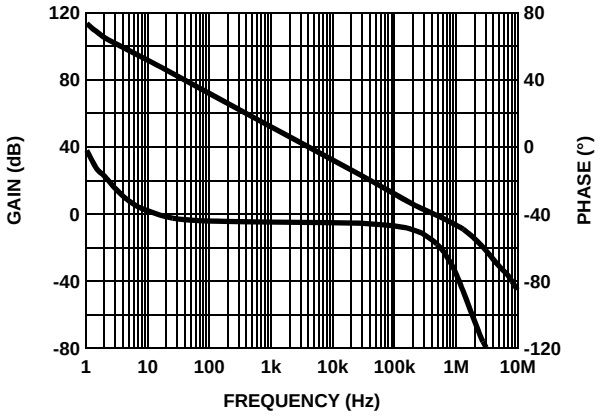


FIGURE 2. A_{VOL} vs FREQUENCY @ 100kΩ LOAD

Typical Performance Curves (Continued)

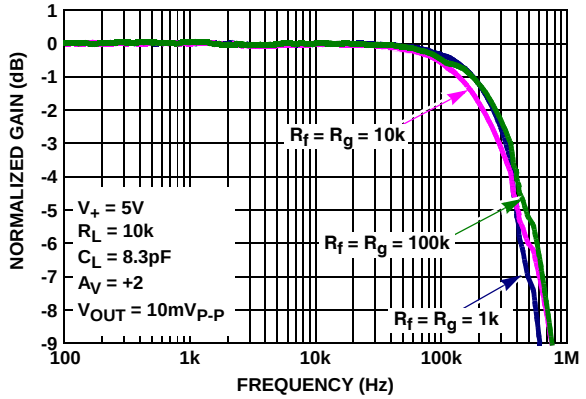


FIGURE 3. GAIN vs FREQUENCY vs FEEDBACK RESISTOR VALUES R_f/R_g

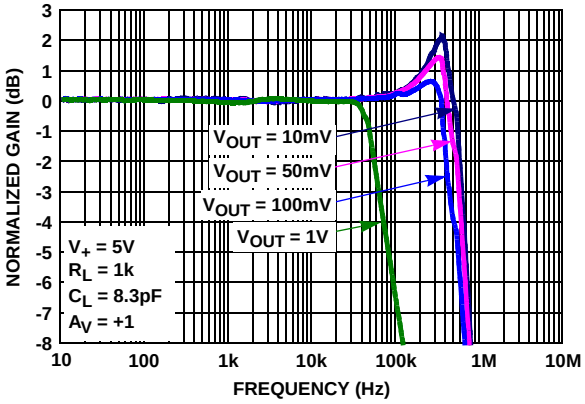


FIGURE 4. GAIN vs FREQUENCY vs V_{OUT}, R_L = 1k

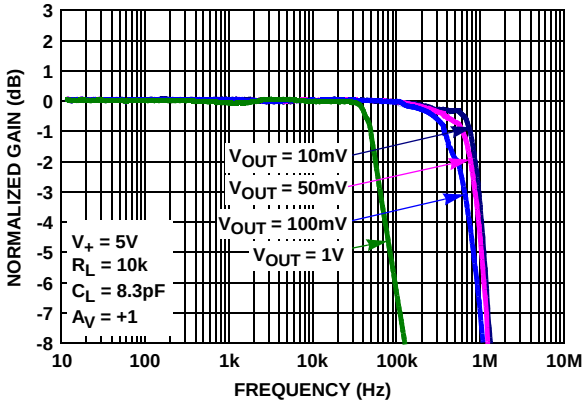


FIGURE 5. GAIN vs FREQUENCY vs V_{OUT}, R_L = 10k

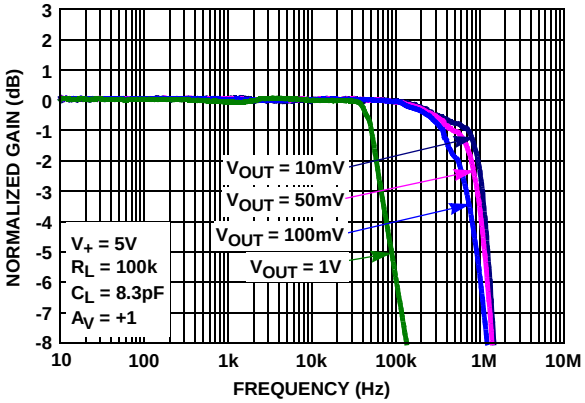


FIGURE 6. GAIN vs FREQUENCY vs V_{OUT}, R_L = 100k

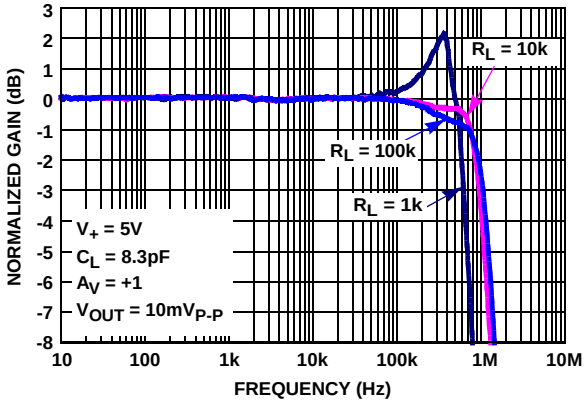


FIGURE 7. GAIN vs FREQUENCY vs R_L

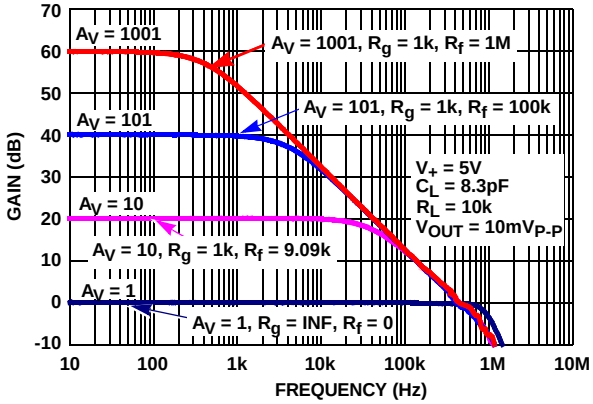


FIGURE 8. FREQUENCY RESPONSE vs CLOSED LOOP GAIN

Typical Performance Curves (Continued)

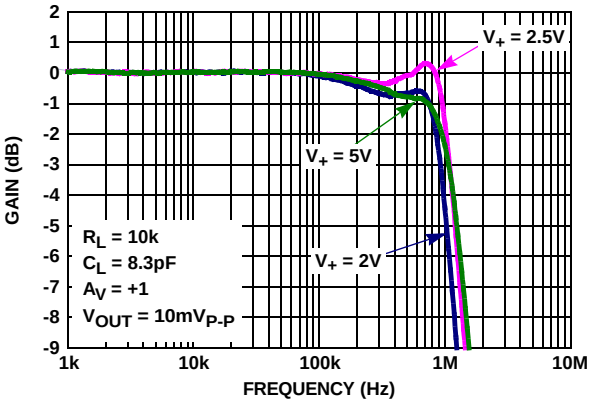


FIGURE 9. GAIN vs FREQUENCY vs SUPPLY VOLTAGE

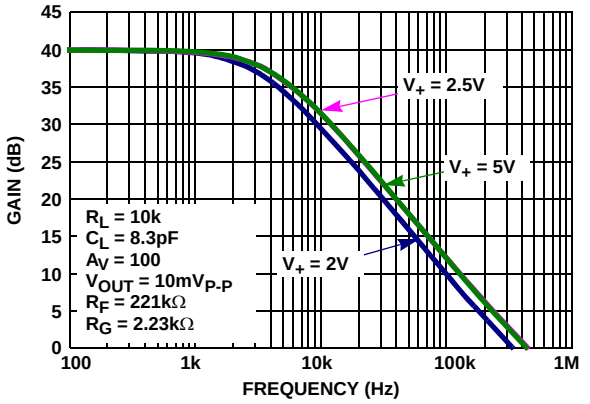


FIGURE 10. GAIN vs FREQUENCY vs SUPPLY VOLTAGE

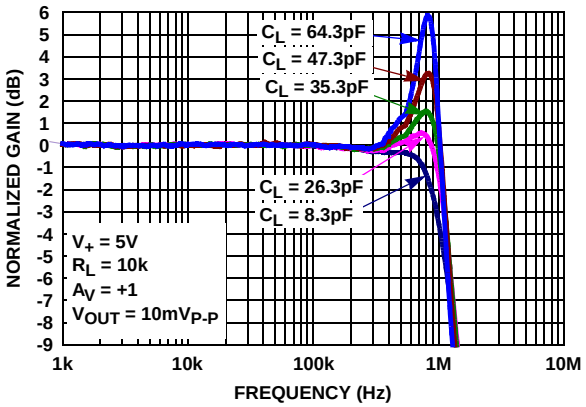


FIGURE 11. GAIN vs FREQUENCY vs C_L

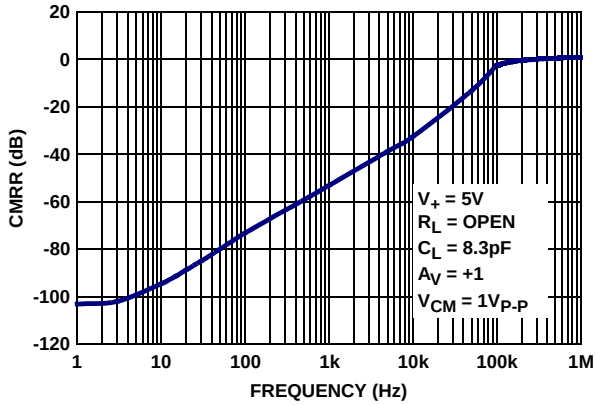


FIGURE 12. CMRR vs FREQUENCY; V_+, V_- = ±2.5V

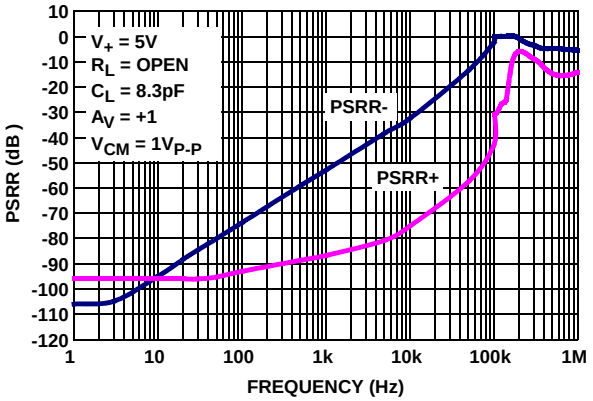


FIGURE 13. PSRR vs FREQUENCY, V_+, V_- = ±2.5V

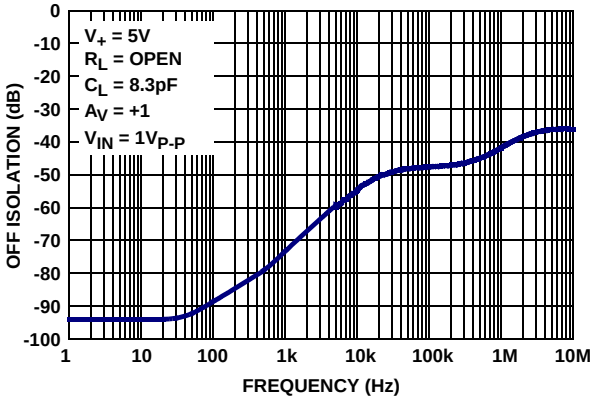


FIGURE 14. OFF ISOLATION vs FREQUENCY; V_+, V_- = ±2.5V

Typical Performance Curves (Continued)

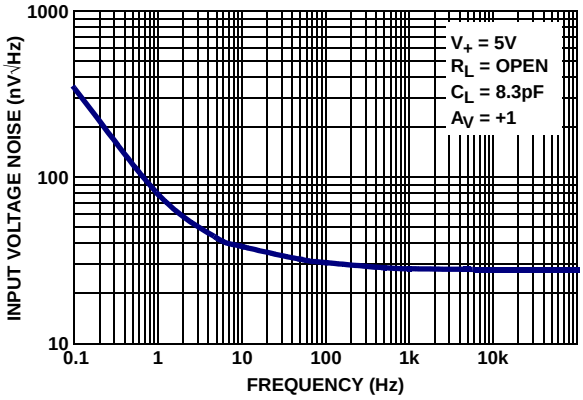


FIGURE 15. INPUT VOLTAGE NOISE DENSITY vs FREQUENCY

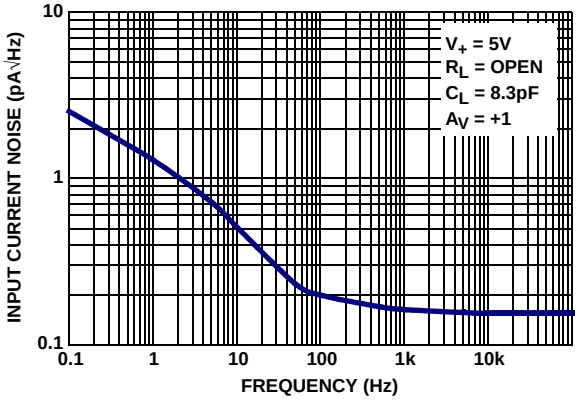


FIGURE 16. INPUT CURRENT NOISE DENSITY vs FREQUENCY

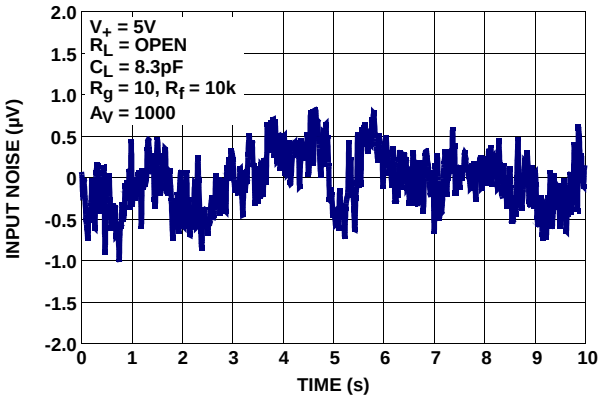


FIGURE 17. INPUT VOLTAGE NOISE 0.1Hz TO 10Hz

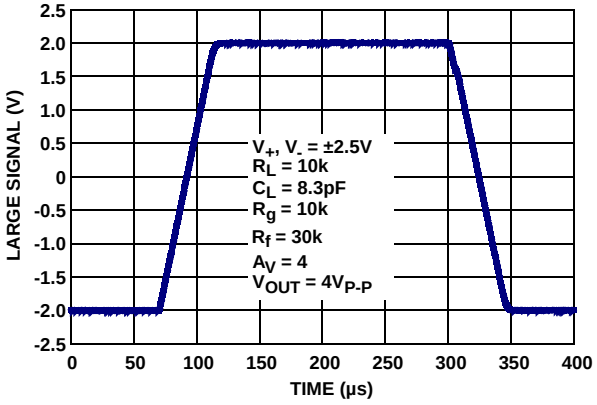


FIGURE 18. LARGE SIGNAL STEP RESPONSE

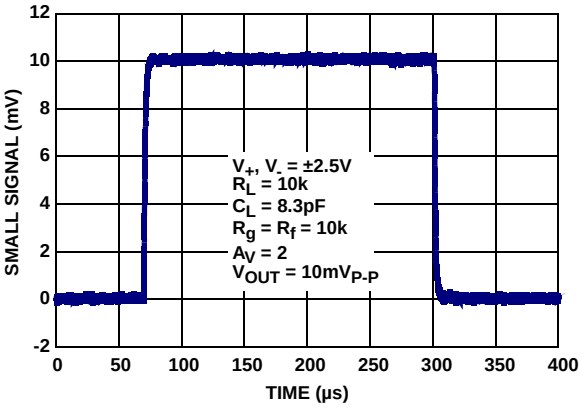


FIGURE 19. SMALL SIGNAL STEP RESPONSE

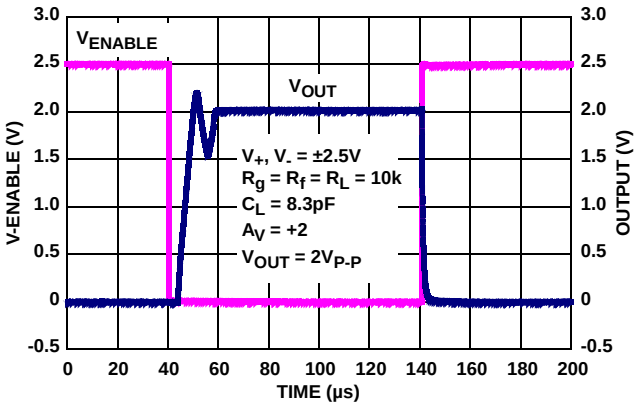


FIGURE 20. ENABLE TO OUTPUT RESPONSE

Typical Performance Curves (Continued)

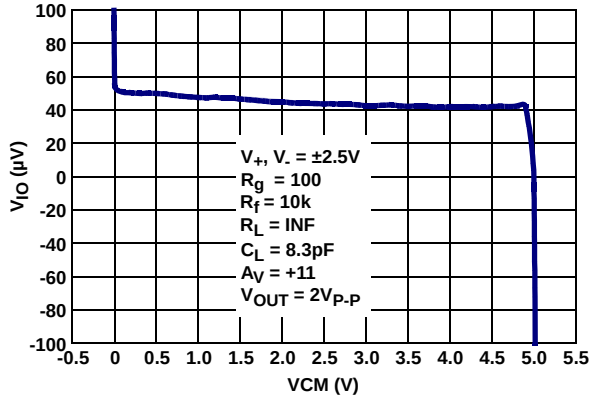


FIGURE 21. INPUT OFFSET VOLTAGE vs COMMON-MODE INPUT VOLTAGE

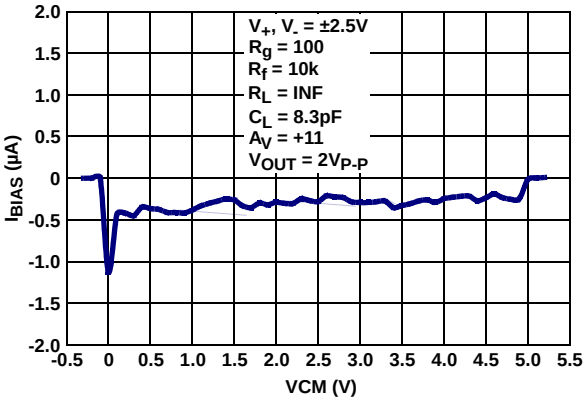


FIGURE 22. INPUT OFFSET CURRENT vs COMMON-MODE INPUT VOLTAGE

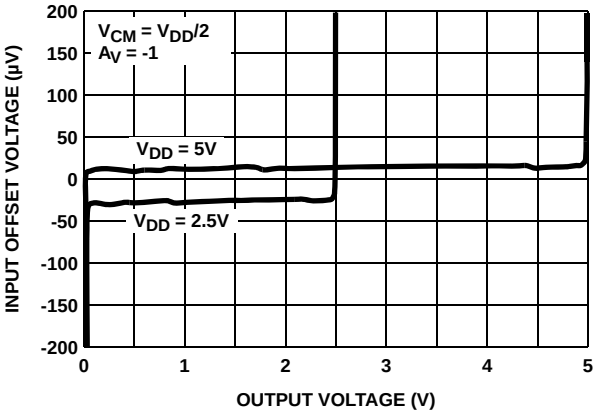


FIGURE 23. INPUT OFFSET VOLTAGE vs OUTPUT VOLTAGE

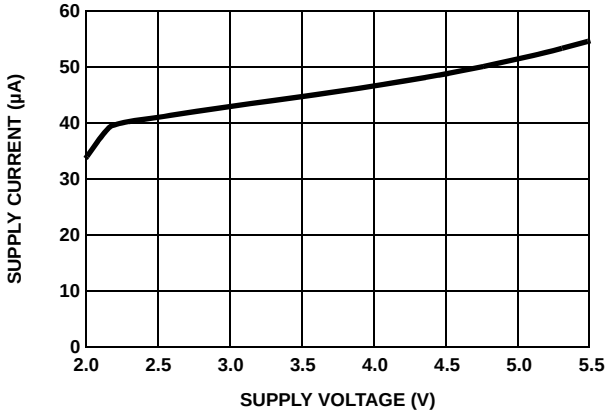


FIGURE 24. SUPPLY CURRENT vs SUPPLY VOLTAGE

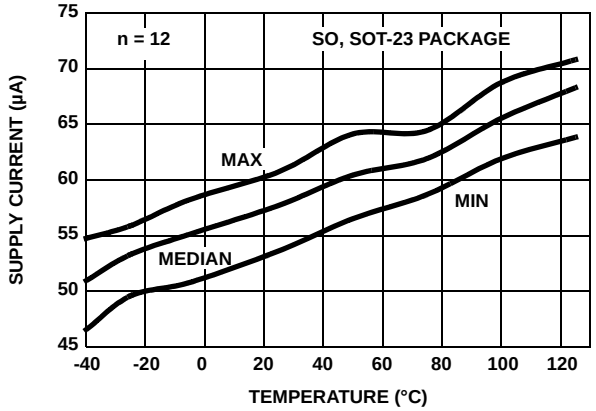


FIGURE 25. SUPPLY CURRENT vs TEMPERATURE V_S = ±2.5V ENABLED. R_L = INF

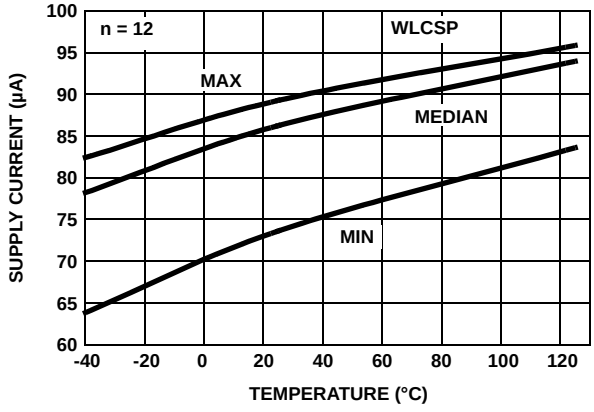


FIGURE 26. SUPPLY CURRENT vs TEMPERATURE V_S = ±2.5V ENABLED. R_L = INF

Typical Performance Curves (Continued)

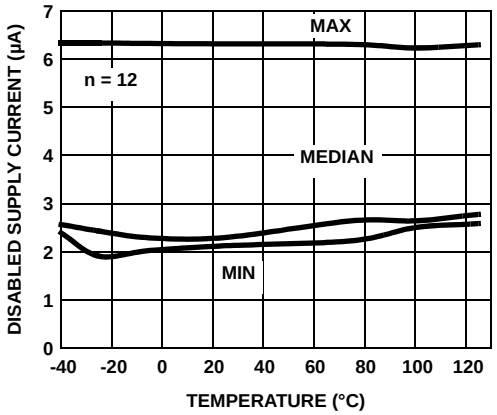


FIGURE 27. DISABLED SUPPLY CURRENT vs TEMPERATURE V_S = ±2.5V R_L= INF

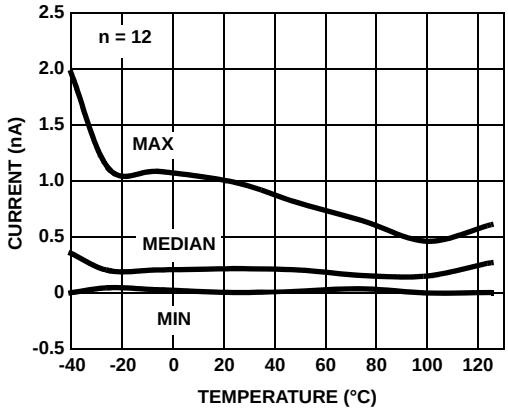


FIGURE 28. I_{BIAS} (+) vs TEMPERATURE V_S = ±2.5V

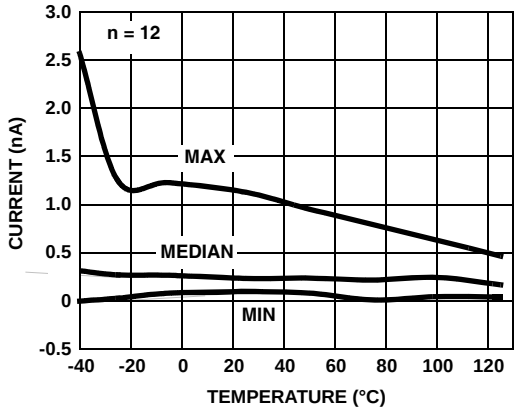


FIGURE 29. I_{BIAS} (+) vs TEMPERATURE V_S = ±1.2V

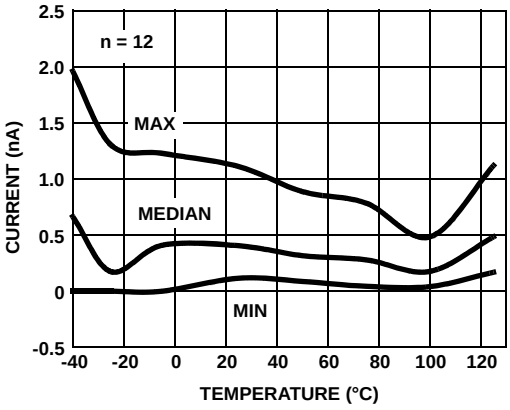


FIGURE 30. I_{BIAS} (-) vs TEMPERATURE V_S = ±2.5V

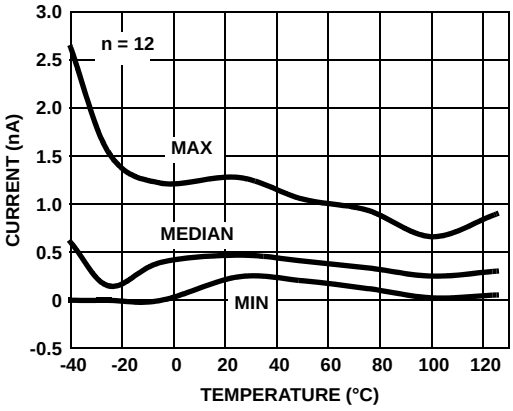


FIGURE 31. I_{BIAS} (-) vs TEMPERATURE V_S = ±1.2V

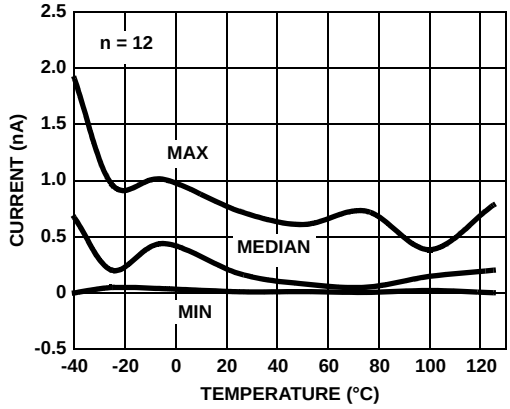


FIGURE 32. INPUT OFFSET CURRENT vs TEMPERATURE V_S = ±2.5V

Typical Performance Curves (Continued)

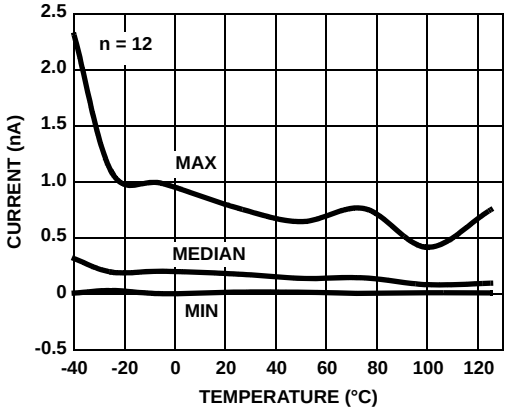


FIGURE 33. INPUT OFFSET CURRENT vs TEMPERATURE
V_S = ±1.2V

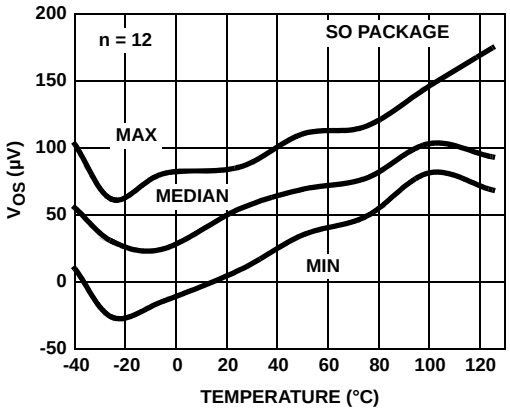


FIGURE 34. INPUT OFFSET VOLTAGE vs TEMPERATURE
V_S = ±2.5V

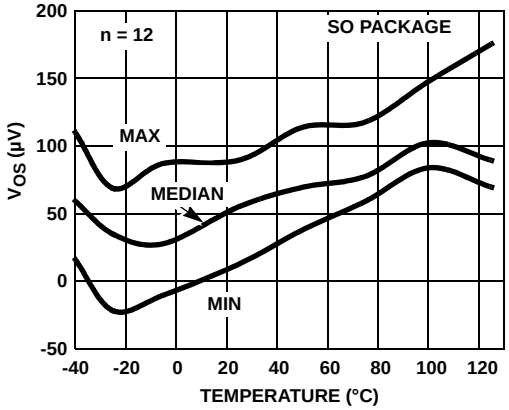


FIGURE 35. INPUT OFFSET VOLTAGE vs TEMPERATURE
V_S = ±1.2V

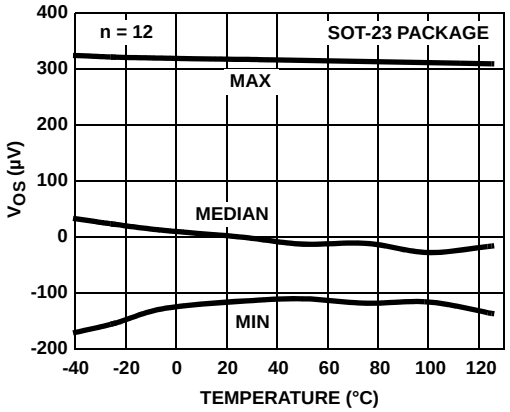


FIGURE 36. INPUT OFFSET VOLTAGE vs TEMPERATURE
V_S = ±2.5V

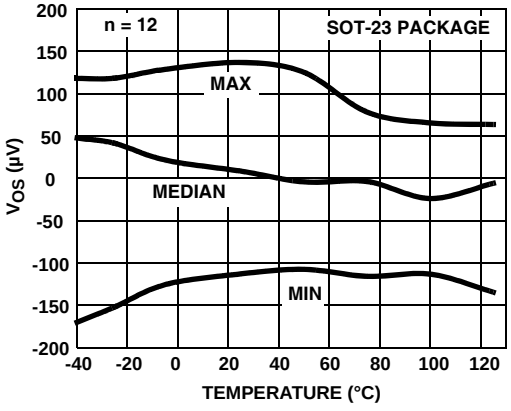


FIGURE 37. INPUT OFFSET VOLTAGE vs TEMPERATURE
V_S = ±1.2V

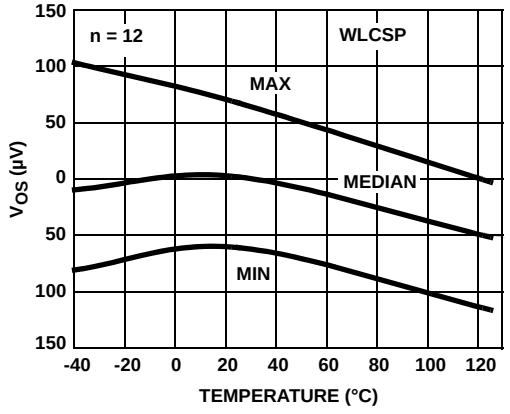


FIGURE 38. INPUT OFFSET VOLTAGE vs TEMPERATURE
V_S = ±2.5V

Typical Performance Curves (Continued)

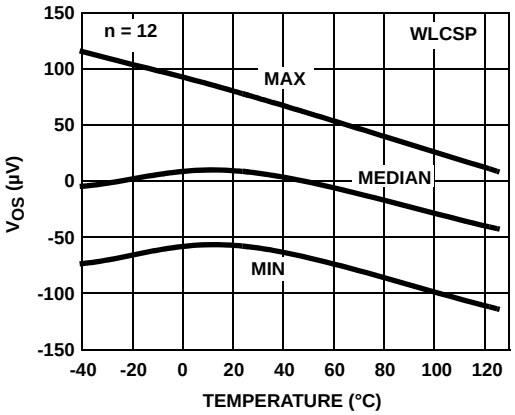


FIGURE 39. INPUT OFFSET VOLTAGE vs TEMPERATURE V_S = ±1.2V

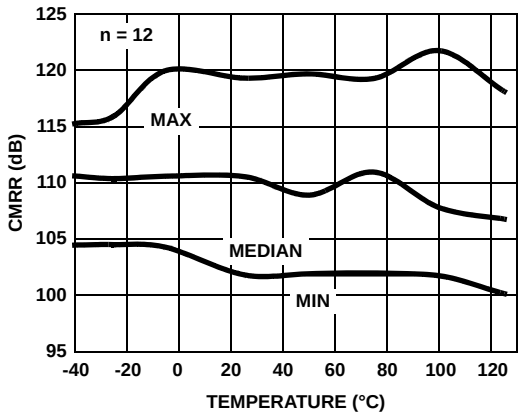


FIGURE 40. CMRR vs TEMPERATURE VCM = +2.5V TO -2.5V

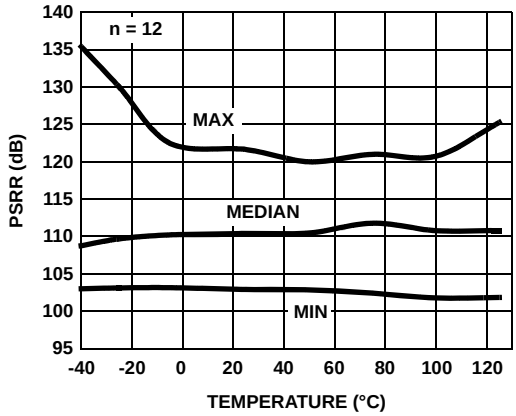


FIGURE 41. PSRR vs TEMPERATURE V_S = ±1.2V TO ±2.5V

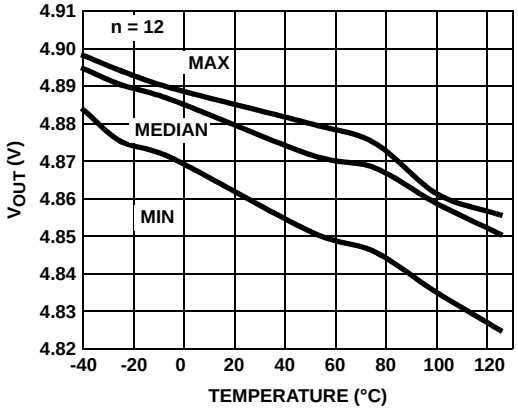


FIGURE 42. POSITIVE V_{OUT} vs TEMPERATURE R_L = 1k V_S = ±2.5V

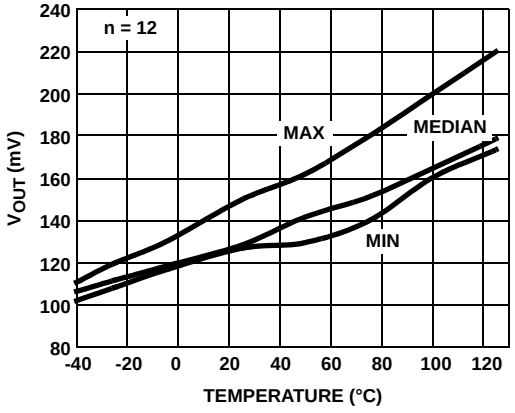


FIGURE 43. NEGATIVE V_{OUT} vs TEMPERATURE R_L = 1k V_S = ±2.5V

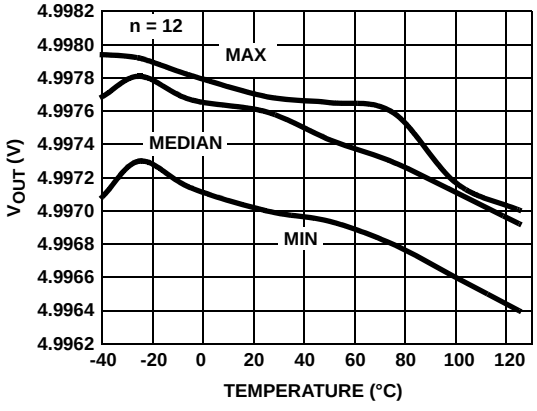


FIGURE 44. POSITIVE V_{OUT} vs TEMPERATURE R_L = 100k V_S = ±2.5V

Typical Performance Curves (Continued)

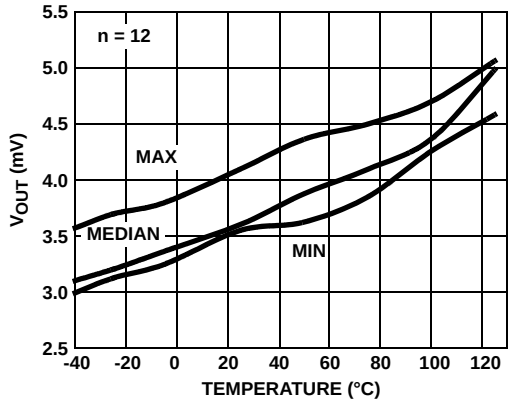


FIGURE 45. NEGATIVE V_{OUT} vs TEMPERATURE R_L = 100k V_S = ±2.5V

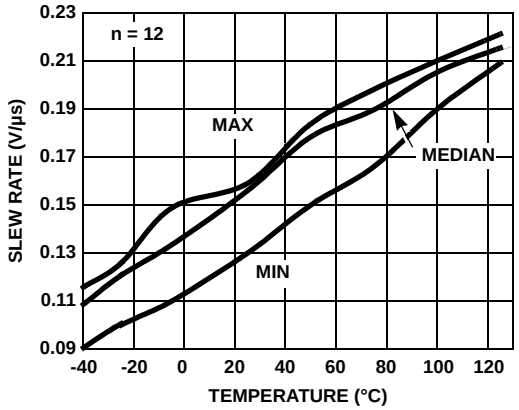


FIGURE 46. +SLEW RATE vs TEMPERATURE V_S = ±2.5V INPUT = ±0.75V, A_V = 2

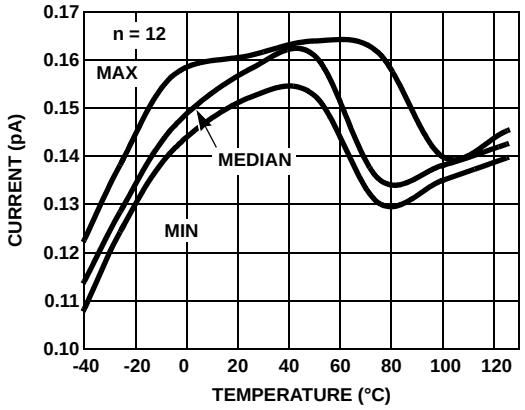


FIGURE 47. -SLEW RATE vs TEMPERATURE V_S = ±2.5V INPUT = ±0.75V, A_V = 2

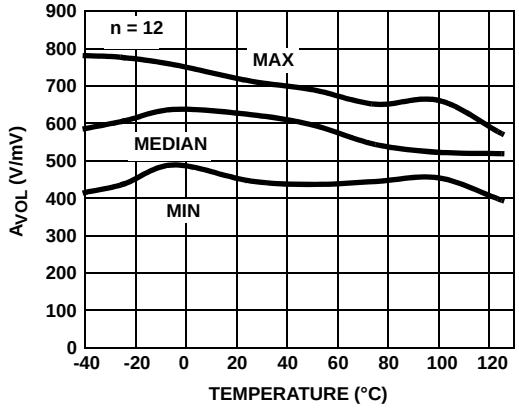
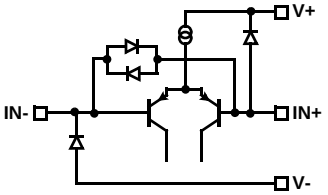


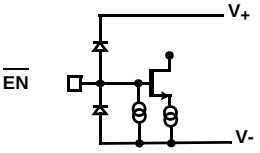
FIGURE 48. A_{VOL}, R_L = 100k, V_S ±2.5V, V_O = ±2V

Pin Descriptions

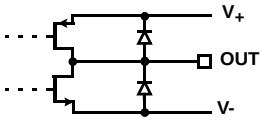
SO PIN NUMBER	SOT-23 PIN NUMBER	6 Ld WLCSP PIN NUMBER	PIN NAME	EQUIVALENT CIRCUIT	DESCRIPTION
1		A1	NC		No internal connection
2	4	C1	IN-	Circuit 1	Amplifier's inverting input
3	3	C2	IN+	Circuit 1	Amplifier's non-inverting input
4	2	B2	V-	Circuit 4	Negative power supply
5			NC		No internal connection
6	1	A2	OUT	Circuit 3	Amplifier's output
7	6	B1	V+	Circuit 4	Positive power supply
8	5		$\overline{EN}$	Circuit 2	Amplifier's enable pin with internal pull-down; Logic "1" selects the disabled state; Logic "0" selects the enabled state.



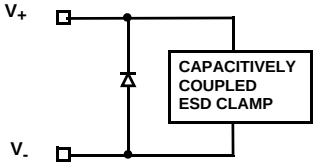
CIRCUIT 1



CIRCUIT 2



CIRCUIT 3



CIRCUIT 4

Applications Information

Introduction

The EL8176 is a rail-to-rail input and output micro-power precision single supply operational amplifier with an enable feature. The device achieves rail-to-rail input and output operation and eliminates the concerns introduced by a conventional rail-to-rail I/O operational amplifier as discussed below.

Rail-to-Rail Input

The input common-mode voltage range of the EL8176 goes from negative supply to positive supply without introducing offset errors or degrading performance associated with a conventional rail-to-rail input operational amplifier. Many rail-to-rail input stages use two differential input pairs, a long-tail PNP (or PFET) and an NPN (or NFET). Severe penalties have to be paid for this circuit topology. As the input signal moves from one supply rail to another, the operational amplifier switches from one input pair to the other causing drastic changes in input offset voltage and an undesired change in magnitude and polarity of input offset current.

The EL8176 achieves input rail-to-rail without sacrificing important precision specifications and without degrading distortion performance. The EL8176's input offset voltage exhibits a smooth behavior throughout the entire common-mode input range. The input bias current versus the common-mode voltage range for the EL8176 gives us an undistorted behavior from typically 10mV above the negative rail all the way up to the positive rail.

Input Bias Current Compensation

The input bias currents as low as 500pA are achieved while maintaining an excellent bandwidth for a micro-power operational amplifier. Inside the EL8176 is an input bias canceling circuit. The input stage transistors are still biased with an adequate current for speed but the canceling circuit sinks most of the base current, leaving a small fraction as input bias current. The input bias current compensation/cancellation is stable from -40°C to +125°C and operates from typically 10mV to the positive supply rail.

Rail-to-Rail Output

A pair of complementary MOSFET devices achieves rail-to-rail output swing. The NMOS sinks current to swing the output in the negative direction. The PMOS sources current to swing the output in the positive direction. The EL8176 with a 100kΩ load will swing to within 3mV of the supply rails.

Enable/Disable Feature

The EL8176 offers an $\overline{EN}$ pin. The active low $\overline{EN}$ pin disables the device when pulled up to at least 2.0V. When disabled, the output is in a high impedance state and the part consumes typically 3µA. When disabled, the high impedance output allows multiple parts to be MUXed together. When configured as a MUX, the outputs are tied together in parallel and a channel can be selected by pulling the $\overline{EN}$ pin to 0.8V or lower.The $\overline{EN}$ pin has an internal pull-down. If left open or floating, the $\overline{EN}$ pin will internally be pulled low, enabling the part by default.

Proper Layout Maximizes Performance

To achieve the maximum performance of the high input impedance and low offset voltage of the EL8176, care should be taken in the circuit board layout. The PC board surface must remain clean and free of moisture to avoid leakage currents between adjacent traces. Surface coating of the circuit board will reduce surface moisture and provide a humidity barrier, reducing parasitic resistance on the board. The use of guard rings around the amplifier inputs will further reduce leakage currents. Figure 49 shows how the guard ring should be configured and Figure 50 shows the top view of how a surface mount layout can be arranged. The guard ring does not need to be a specific width, but it should form a continuous loop around both inputs. By setting the guard ring voltage equal to the voltage at the non-inverting input, parasitic capacitance is minimized as well. For further reduction of leakage currents, components can be mounted to the PC board using Teflon standoff insulators.

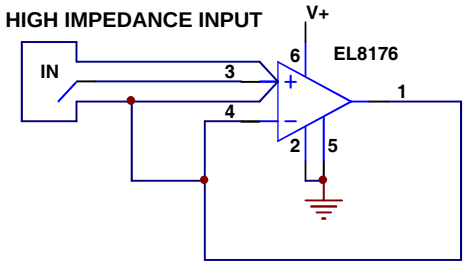


FIGURE 49.

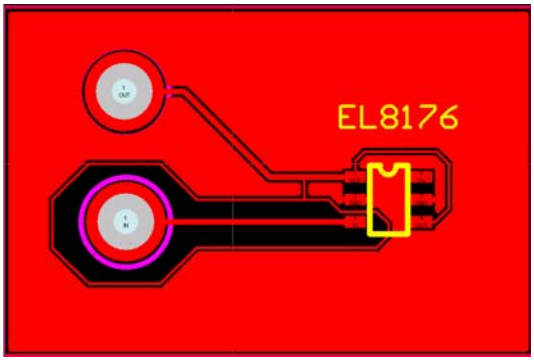


FIGURE 50.

Typical Applications

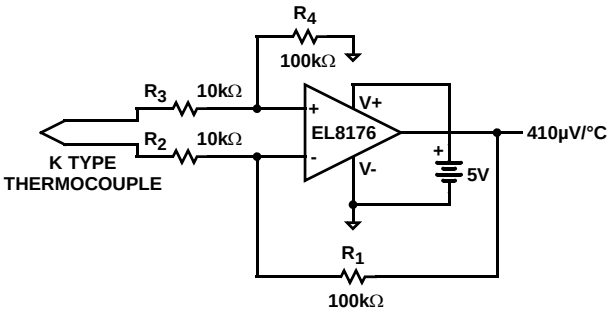
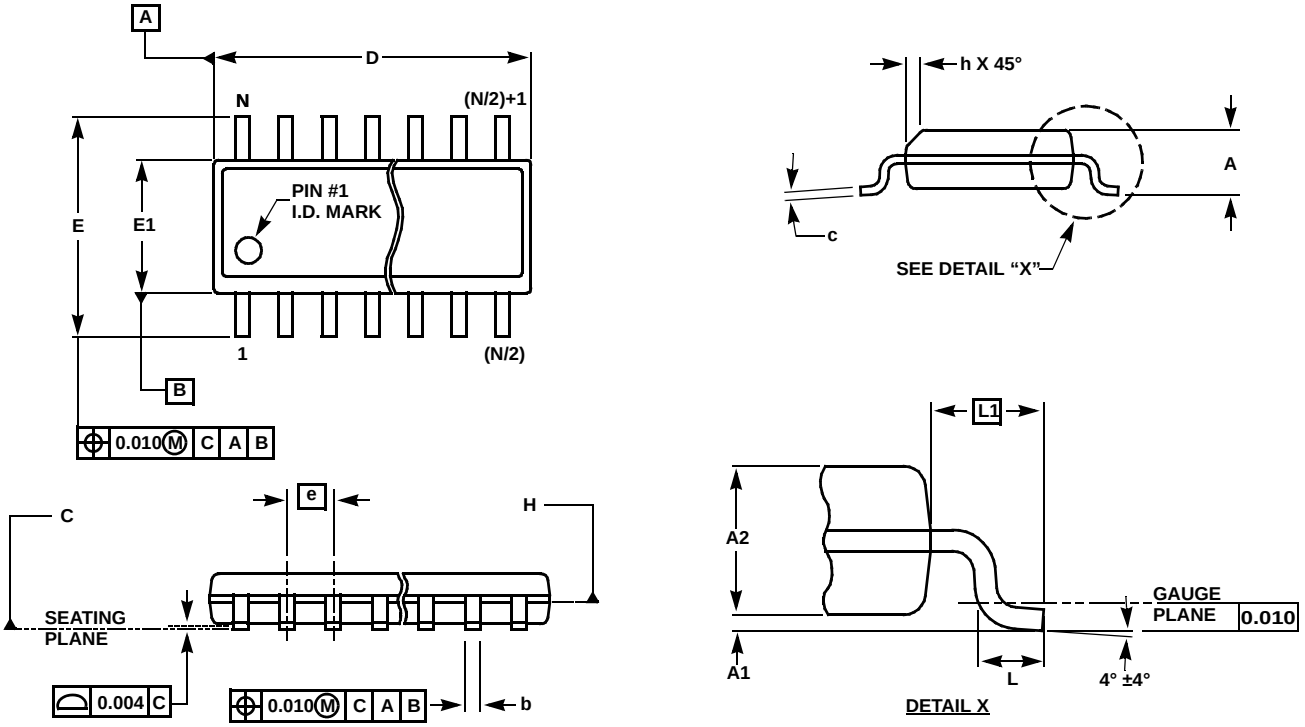


FIGURE 51. THERMOCOUPLE AMPLIFIER

Thermocouples are the most popular temperature-sensing device because of their low cost, interchangeability, and ability to measure a wide range of temperatures. The EL8176 is used to convert the differential thermocouple voltage into single-ended signal with 10X gain. The EL8176's rail-to-rail input characteristic allows the thermocouple to be biased at ground and the converter to run from a single 5V supply.

Small Outline Package Family (SO)



MDP0027

SMALL OUTLINE PACKAGE FAMILY (SO)

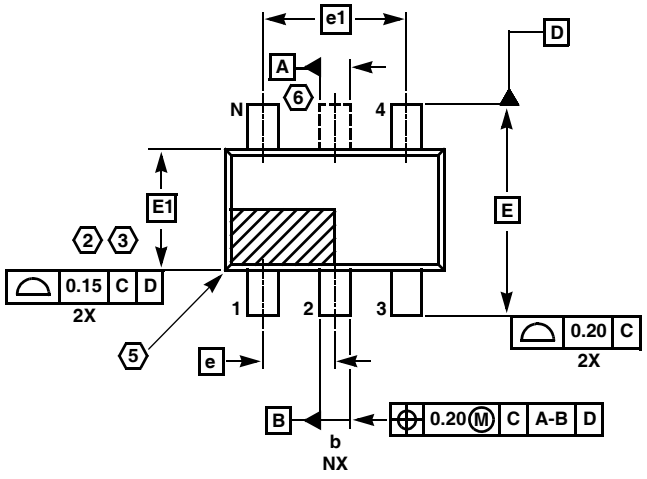
SYMBOL	INCHES							TOLERANCE	NOTES
	SO-8	SO-14	SO16 (0.150")	SO16 (0.300") (SOL-16)	SO20 (SOL-20)	SO24 (SOL-24)	SO28 (SOL-28)		
A	0.068	0.068	0.068	0.104	0.104	0.104	0.104	MAX	-
A1	0.006	0.006	0.006	0.007	0.007	0.007	0.007	±0.003	-
A2	0.057	0.057	0.057	0.092	0.092	0.092	0.092	±0.002	-
b	0.017	0.017	0.017	0.017	0.017	0.017	0.017	±0.003	-
c	0.009	0.009	0.009	0.011	0.011	0.011	0.011	±0.001	-
D	0.193	0.341	0.390	0.406	0.504	0.606	0.704	±0.004	1, 3
E	0.236	0.236	0.236	0.406	0.406	0.406	0.406	±0.008	-
E1	0.154	0.154	0.154	0.295	0.295	0.295	0.295	±0.004	2, 3
e	0.050	0.050	0.050	0.050	0.050	0.050	0.050	Basic	-
L	0.025	0.025	0.025	0.030	0.030	0.030	0.030	±0.009	-
L1	0.041	0.041	0.041	0.056	0.056	0.056	0.056	Basic	-
h	0.013	0.013	0.013	0.020	0.020	0.020	0.020	Reference	-
N	8	14	16	16	20	24	28	Reference	-

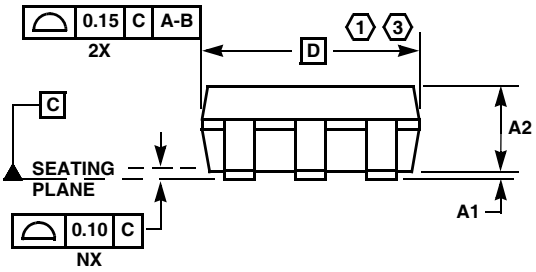
Rev. M 2/07

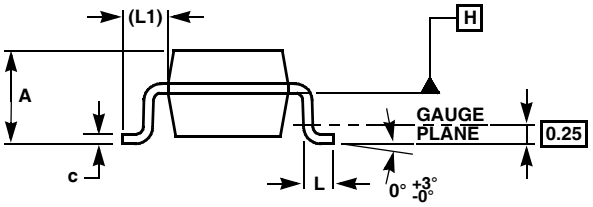
NOTES:

1. Plastic or metal protrusions of 0.006" maximum per side are not included.
2. Plastic interlead protrusions of 0.010" maximum per side are not included.
3. Dimensions "D" and "E1" are measured at Datum Plane "H".
4. Dimensioning and tolerancing per ASME Y14.5M-1994

SOT-23 Package Family







MDP0038

SOT-23 PACKAGE FAMILY

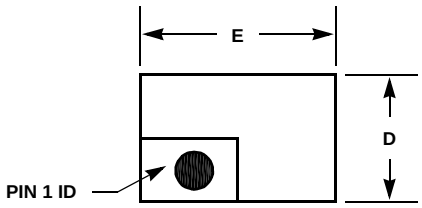
SYMBOL	MILLIMETERS		TOLERANCE
	SOT23-5	SOT23-6	
A	1.45	1.45	MAX
A1	0.10	0.10	±0.05
A2	1.14	1.14	±0.15
b	0.40	0.40	±0.05
c	0.14	0.14	±0.06
D	2.90	2.90	Basic
E	2.80	2.80	Basic
E1	1.60	1.60	Basic
e	0.95	0.95	Basic
e1	1.90	1.90	Basic
L	0.45	0.45	±0.10
L1	0.60	0.60	Reference
N	5	6	Reference

Rev. F 2/07

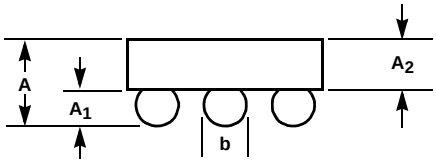
NOTES:

1. Plastic or metal protrusions of 0.25mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25mm maximum per side are not included.
3. This dimension is measured at Datum Plane “H”.
4. Dimensioning and tolerancing per ASME Y14.5M-1994.
5. Index area - Pin #1 I.D. will be located within the indicated zone (SOT23-6 only).
6. SOT23-5 version has no center lead (shown as a dashed line).

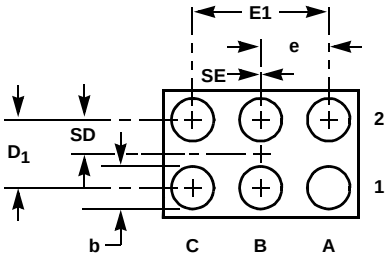
Wafer Level Chip Scale Package (WLCSP)



TOP VIEW



SIDE VIEW



BOTTOM VIEW

W3x2.6C

3x2 ARRAY 6 BALL WAFER LEVEL CHIP SCALE PACKAGE

SYMBOL	MILLIMETERS
A	0.51 Min, 0.55 Max
A_1	0.225 ±0.015
A_2	0.305 ±0.013
b	Φ0.323 ±0.025
D	0.955 ±0.020
D_1	0.50 BASIC
E	1.455 ±0.020
E_1	1.00 BASIC
e	0.50 BASIC
SD	0.25 BASIC
SE	0.00 BASIC

Rev. 3 03/08

NOTES:

1. All dimensions are in millimeters.